CLAIMS

I claim:

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1. A method for transmitting Packetized SCSI Protocol command blocks comprising:

transmitting a first Packetized SCSI Protocol command block; and

transmitting a second Packetized SCSI Protocol command block with a substantially zero latency following transmission of said first Packetized SCSI Protocol command block.

2. The method of Claim 1 wherein transmitting said first Packetized SCSI Protocol command block further comprises:

transmitting at least one byte in said first Packetized SCSI Protocol command block directly from a storage location of said at least one byte.

3. The method of Claim 2 wherein said storage location of said at least one byte is within a stored first hardware I/O control block.

4. The method of Claim 3 wherein said at least one byte is in a logical unit number field of said first Packetized SCSI protocol command block.

5. The method of Claim 2 wherein said storage location of said at least one byte is within a pointer register of a host adapter integrated circuit.

6. The method of Claim 3 wherein said stored first hardware I/O control block includes a pointer to a storage location of a second hardware I/O control

block, and further wherein said second hardware I/O control block includes information used directly in said transmitting said second Packetized SCSI Protocol command block.

7. A SCSI initiator system comprising:

a target execution queue containing at least two hardware I/O control blocks for a SCSI target wherein the target execution queue is stored in a memory; and

a Packetized SCSI Protocol hardware packet engine coupled to the target execution queue, wherein the Packetized SCSI Protocol hardware packet engine transmits a Packetized SCSI Protocol command block for each hardware I/O control block in said target execution queue with substantially zero latency between transmission of adjacent Packetized SCSI Protocol command blocks.

8. The SCSI initiator system of Claim 7 wherein the Packetized SCSI protocol hardware packet engine further comprise:

a hardware information unit transfer controller having a start input line and a data out phase input line wherein the hardware information unit transfer controller sequences hardware generation of the Packetized SCSI Protocol command blocks upon receiving an active signal on the start input line and an active signal on the data out phase input line.

9. The SCSI initiator system of Claim 8 wherein the Packetized SCSI protocol hardware packet engine further comprises:

a hardware header generator coupled to the hardware information unit transfer controller, wherein the hardware header generator generates fields in a command L_Q information unit in response to signals from the hardware information unit transfer controller.

10. The SCSI initiator system of Claim 8 wherein the Packetized SCSI protocol hardware packet engine further comprises:

a hardware body generator coupled to the hardware information unit transfer controller, wherein the hardware header generator generates fields in a command information unit in response to signals from the hardware information unit transfer controller.

11. The SCSI initiator system of Claim 9 wherein the Packetized SCSI protocol hardware packet engine further comprises:

a hardware body generator coupled to the hardware information unit transfer controller, wherein the hardware body generator generates fields in a command information unit in response to signals from the hardware information unit transfer controller.

12. The SCSI initiator system of Claim 9 further comprising a hardware I/O control block pointer register coupled to the hardware header generator.

13. The SCSI initiator system of Claim 10 further comprising a hardware I/O control block pointer register coupled to the hardware body generator.

14. The SCSI initiator system of Claim 11 further comprising a hardware I/O control block pointer register coupled to the hardware header generator.

15. The SCSI initiator system of Claim 14 wherein the hardware I/O control block pointer register is also coupled to the hardware body generator.

16. A Packetized SCSI Protocol hardware packet engine comprising:

a hardware information unit transfer controller having a start input line and a data out phase input line wherein the information unit transfer controller sequences hardware generation of a Packetized SCSI Protocol packet byte stream upon receipt of an active signal on the start input line and an active signal on the data out phase input line; and

a hardware header generator coupled to the hardware information unit transfer controller, wherein the hardware header generator generates fields in a command L_Q information unit in response to signals from the hardware information unit transfer controller.

17. The Packetized SCSI Protocol hardware packet engine of Claim 16 further comprising:

a hardware body generator coupled to the hardware information unit transfer controller, wherein the hardware header generator generates fields in a command information unit in response to signals from the hardware information unit transfer controller.

18. The Packetized SCSI Protocol hardware packet engine of Claim 17 further comprising a hardware I/O control block pointer register coupled to the hardware header generator.

19. The Packetized SCSI Protocol hardware packet engine of Claim 17 further comprising a hardware I/O control block pointer register coupled to the hardware body generator.

20. The Packetized SCSI Protocol hardware packet engine of Claim 17 further comprising a hardware I/O control block pointer register coupled to the hardware header generator.

21. A method for generating a Packetized SCSI Protocol command block comprising:

transferring information required in a command information unit and available in a hardware I/O control block directly from the hardware I/O control block; and

transferring information required in the command information unit but unavailable in the hardware I/O control block directly from a register.